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Inventor Information for 10/687437

Inventor Name	City	State/Country
DHONG, SANG HOO	AUSTIN	TEXAS
MUELLER, SILVIA MELITTA	ST. INGBERT	GERMANY
NISHIKAWA, HIROO	SHIGA	JAPAN
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Application#	Patent#	Status	Date Filed	Title	Inventor Name
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09075918	6212619	150	05/11/1998	SYSTEM AND METHOD FOR HIGH-SPEED REGISTER RENAMING BY COUNTING USING TABLE HAVING REGISTER BITS FOR EACH INSTRUCTION IN FLIGHT	DHONG, SANG HOO
09096755	Not Issued	161	06/12/1998	MULTIFUNCTIONAL MACRO	DHONG, SANG HOO
09114117	6175852	250	07/13/1998	HIGH-SPEED BINARY ADDER	DHONG, SANG HOO
09139940	6178437	250	08/25/1998	METHOD AND APPARATUS FOR ANTICIPATING LEADING DIGITS AND NORMALIZATION SHIFT AMOUNTS IN A FLOATING-POINT PROCESSOR	DHONG, SANG HOO
09149229	6226731	150	09/08/1998	METHOD AND SYSTEM FOR ACCESSING A CACHE MEMORY WITHIN A DATA-PROCESSING SYSTEM UTILIZING A PRE-CALCULATED COMPARISON ARRAY	DHONG, SANG HOO

09182593	6345286	150	10/30/1998	A 6-TO-3 CARRY-SAVE ADDER	DHONG, SANG HOO
09187340	6076140	150	11/06/1998	SET ASSOCIATIVE CACHE MEMODRY SYSTEM WITH REDUCED POWER CONSUMPTION	DHONG, SANG HOO
09207482	6237085	250	12/08/1998	PROCESSOR AND METHOD FOR GENERATING LESS THAN (LT), GREATER THAN (GT), AND EQUAL TO (EQ) CONDITION CODE BITS CONCURRENT WITH A LOGICAL OR COMPLEX OPERATION	DHONG, SANG HOO
09207483	6282557	250	12/08/1998	LOW LATENCY FUSED MULTIPLY-ADDER	DHONG, SANG HOO
09244079	6021461	150	02/04/1999	METHOD FOR REDUCING POWER CONSUMPTION IN A SET ASSOCIATIVE CACHE MEMORY SYSTEM	DHONG, SANG HOO
09263031	6221769	150	03/05/1999	METHOD FOR INTEGRATED CIRCUIT POWER AND ELECTRICAL CONNECTIONS VIA THROUGH-WAFER INTERCONNECTS	DHONG, SANG HOO
09263032	6268660	150	03/05/1999	SILICON PACKAGING WITH THROUGH WAFER INTERCONNECTS	DHONG, SANG HOO
09270469	6360238	150	03/15/1999	A LEADING ZERO /ONE ANTICIPATOR HAVING AN INTEGRATED SIGN SELECTOR	DHONG, SANG HOO
09272489	6421699	150	03/19/1999	METHOD AND SYSTEM FOR A SPEEDUP OF A BIT-MULTIPLIER	DHONG, SANG HOO
09290921	6166437	150	04/12/1999	SILICON ON SILICON PACKAGE WITH PRECISION ALIGN MACRO	DHONG, SANG HOO
09343450	6393446	150	06/30/1999	32-BIT AND 64-BIT DUAL MODE ROTATOR	DHONG, SANG HOO
09404283	Not Issued	168	09/23/1999	HIGH-SPEED DYNAMIC MULTI-BIT COMPARATOR AND ARRAY ARCHITECTURE	DHONG, SANG HOO
09418377	6232872	250	10/14/1999	COMPARATOR	DHONG, SANG HOO
09438614	Not Issued	168	11/12/1999	LOW-POWER DYNAMIC LOGIC CIRCUIT	DHONG, SANG HOO
09440758	6292027	150	11/16/1999	FAST LOW-POWER LOGIC GATES AND METHOD FOR EVALUATING LOGIC SIGNALS	DHONG, SANG HOO
09443205	6294929	150	11/18/1999	BALANCED-DELAY PROGRAMMABLE LOGIC ARRAY AND METHOD FOR BALANCING PROGRAMMABLE LOGIC ARRAY DELAYS	DHONG, SANG HOO
09450982	6239620	150	11/29/1999	METHOD AND APPARATUS FOR	DHONG, SANG HOO

				GENERATING TRUE/COMPLEMENT SIGNALS	
09457938	6232798	150	12/09/1999	SELF-RESETTING CIRCUIT TIMING CORRECTION	DHONG, SANG HOO
09458405	6453390	150	12/10/1999	PROCESSOR CYCLE TIME INDEPENDENT PIPELINE CACHE AND METHOD FOR PIPELINING DATA FROM A CACHE	DHONG, SANG HOO
09465176	6453258	150	12/17/1999	OPTIMIZED BURN-IN FOR FIXED TIME DYNAMIC LOGIC CIRCUITRY	DHONG, SANG HOO
10273590	6717882	150	10/17/2002	CELL CIRCUIT FOR MULTIPORT MEMORY USING 3-WAY MULTIPLEXER	DHONG, SANG HOO
10687437	Not Issued	30	10/16/2003	Methods and apparatus for performing multi-value range checks	DHONG, SANG HOO
10937693	Not Issued	30	09/09/2004	Construction of a folded leading zero anticipator	DHONG, SANG HOO

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Inventor Name Search Result

Your Search was:

Last Name = MUELLER
First Name = SILVIA

Application#	Patent#	Status	Date Filed	Title	Inventor Name
11459663	Not Issued	25	07/25/2006	Leading-Zero Counter and Method to Count Leading Zeros	MUELLER, SILVIA
11462069	Not Issued	20	08/03/2006	Method and Processor for Performing a Floating-Point Instruction Within a Processor	MUELLER, SILVIA
10821606	Not Issued	30	04/08/2004	Fast operand formatting for a high performance multiply-add floating point-unit	MUELLER, SILVIA M.
10392764	7058830	150	03/19/2003	POWER SAVING IN A FLOATING POINT UNIT USING A MULTIPLIER AND ALIGNER BYPASS	MUELLER, SILVIA MELITTA
10439037	7137021	150	05/15/2003	POWER SAVING IN FPU WITH GATED POWER BASED ON OPCODES AND DATA	MUELLER, SILVIA MELITTA
10621908	7149877	150	07/17/2003	BYTE EXECUTION UNIT FOR CARRYING OUT BYTE INSTRUCTIONS IN A PROCESSOR	MUELLER, SILVIA MELITTA
10687437	Not Issued	30	10/16/2003	Methods and apparatus for performing multi-value range checks	MUELLER, SILVIA MELITTA
10718303	Not Issued	30	11/20/2003	High performance implementation of exponent adjustment in a floating point design	MUELLER, SILVIA MELITTA
10733839	Not Issued	41	12/11/2003	High speed adder design for a multiply-add based floating point unit	MUELLER, SILVIA MELITTA
10891771	Not Issued	41	07/15/2004	Protecting one-hot logic against short-curcuits during power-on	MUELLER, SILVIA MELITTA
10902475	Not Issued	30	07/29/2004	Apparatus and method for reducing the latency of sum-addressed shifters	MUELLER, SILVIA MELITTA
10912480	Not Issued	30	08/05/2004	Alignment shifter supporting multiple precisions	MUELLER, SILVIA MELITTA
10982110	Not Issued	30	11/05/2004	Apparatus for controlling rounding modes in single instruction multiple data (SIMD) floating-point units	MUELLER, SILVIA MELITTA
10982111	Not Issued	71	11/05/2004	Leakage current reduction system and method	MUELLER, SILVIA MELITTA
10982119	Not Issued	30	11/05/2004	Using a leading-sign anticipator circuit for detecting sticky-bit information	MUELLER, SILVIA MELITTA

11055812	Not Issued	30	02/11/2005	Floating point unit with fused multiply add and method for calculating a result with a floating point unit	MUELLER, SILVIA MELITTA
11127848	Not Issued	41	05/12/2005	Processor having efficient function estimate instructions	MUELLER, SILVIA MELITTA
11555513	Not Issued	25	11/01/2006	Byte Execution Unit for Carrying Out Byte Instructions in a Processor	MUELLER, SILVIA MELITTA
10937693	Not Issued	30	09/09/2004	Construction of a folded leading zero anticipator	MUELLER, SILVIA MELITTA

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Inventor Name Search Result

Your Search was:

Last Name = NISHIKAWA
First Name = HIROO

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10687437	Not Issued	30	10/16/2003	Methods and apparatus for performing multi-value range checks	NISHIKAWA, HIROO
10821606	Not Issued	30	04/08/2004	Fast operand formatting for a high performance multiply-add floating point-unit	NISHIKAWA, HIROO
10902475	Not Issued	30	07/29/2004	Apparatus and method for reducing the latency of sum-addressed shifters	NISHIKAWA, HIROO

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Your Search was:

Last Name = OH
First Name = HWA-JOON

Application#	Patent#	Status	Date Filed	Title	Inventor Name
08430542	5689621	150	04/28/1995	MODULAR FEEDFORWARD NEURAL NETWORK ARCHITECTURE WITH LEARNING	OH, HWA-JOON
09843504	6829682	150	04/26/2001	DESTRUCTIVE READ ARCHITECTURE FOR DYNAMIC RANDOM ACCESS MEMORIES	OH, HWA-JOON
09844837	6587388	150	04/27/2001	METHOD AND APPARATUS FOR REDUCING WRITE OPERATION TIME IN DYNAMIC RANDOM ACCESS MEMORIES	OH, HWA-JOON
09982163	6510093	150	10/18/2001	METHOD AND APPARATUS FOR CYCLE TIME REDUCTION IN A MEMORY SYSTEM USING ALTERNATING REFERENCE CELLS AND ISOLATED SENSE LINES	OH, HWA-JOON
10392764	7058830	150	03/19/2003	POWER SAVING IN A FLOATING POINT UNIT USING A MULTIPLIER AND ALIGNER BYPASS	OH, HWA-JOON
10439037	7137021	150	05/15/2003	POWER SAVING IN FPU WITH GATED POWER BASED ON OPCODES AND DATA	OH, HWA-JOON
10616850	6914453	150	07/10/2003	INTEGRATED LOGIC AND LATCH DESIGN WITH CLOCK GATING AT STATIC INPUT SIGNALS	OH, HWA-JOON
10621908	7149877	150	07/17/2003	BYTE EXECUTION UNIT FOR CARRYING OUT BYTE INSTRUCTIONS IN A PROCESSOR	OH, HWA-JOON
10687437	Not Issued	30	10/16/2003	Methods and apparatus for performing multi-value range checks	OH, HWA-JOON
10718303	Not Issued	30	11/20/2003	High performance implementation of exponent adjustment in a floating point design	OH, HWA-JOON
10733839	Not Issued	41	12/11/2003	High speed adder design for a multiply-add based floating point unit	OH, HWA-JOON
10821606	Not Issued	30	04/08/2004	Fast operand formatting for a high performance multiply-add floating point-unit	OH, HWA-JOON
10891771	Not	41	07/15/2004	Protecting one-hot logic against short-	OH, HWA-JOON

	Issued			curcuits during power-on	
10902475	Not Issued	30	07/29/2004	Apparatus and method for reducing the latency of sum-addressed shifters	OH, HWA-JOON
10912480	Not Issued	30	08/05/2004	Alignment shifter supporting multiple precisions	OH, HWA-JOON
10937693	Not Issued	30	09/09/2004	Construction of a folded leading zero anticipator	OH, HWA-JOON
10982110	Not Issued	30	11/05/2004	Apparatus for controlling rounding modes in single instruction multiple data (SIMD) floating-point units	OH, HWA-JOON
10982111	Not Issued	71	11/05/2004	Leakage current reduction system and method	OH, HWA-JOON
10982119	Not Issued	30	11/05/2004	Using a leading-sign anticipator circuit for detecting sticky-bit information	OH, HWA-JOON
11127848	Not Issued	41	05/12/2005	Processor having efficient function estimate instructions	OH, HWA-JOON
11555513	Not Issued	25	11/01/2006	Byte Execution Unit for Carrying Out Byte Instructions in a Processor	OH, HWA-JOON

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Filtering on **range** and **multi-value** parameters has a few idiosyncrasies that you need ... The first task is to **check** if the Output string has a value from a ...
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Swapping **Multi-Value** Field Values · Looping to perform lookups ... But then the next statement should **check** for a number and the **range**. ...
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Servers and Processes
Anti-spamming **check**. **Range**: **multi-value**. Default Value: none. Recipient Rewriting Rules. This parameter rewrites rules for recipients. **Range**: **multi-value** ...
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All **MultiValue** databases support a **range** of APIs that allow to them to ... **Check** the Web Links on this site for vendors, **check** the IBM Website for docs on ...
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